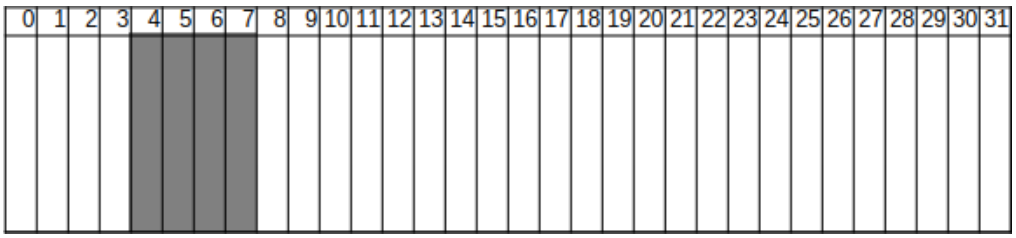
1. In the following diagram of a 4-way set-associative cache with 32 blocks, highlight the areas of the cache where block 17 can be placed.



2. Calculate the number of bits required for the *index*, *offset*, *tag* for a *direct-mapped cache* with **1024 cache lines** and **32 bytes per line**.

$L = 1024$ (given). $W = 1$ because it's direct-mapped. $B = 32$ (given).

$$\text{Index bits} = \log_2\left(\frac{1024}{1}\right) = 10$$
$$\text{Offset bits} = \log_2(32) = 5$$
$$\text{Tag bits} = 32 - (10 + 5) = 17$$

3. Calculate the number of bits required for the *index*, *offset*, and *tag* for a **32 KiB direct-mapped cache** with **64-byte cache lines**.

$L = 32\text{KiB}/64\text{B} = 512$ (cache size over line size). $W = 1$ because it's direct-mapped. $B = 64$ (given).

$$\text{Index bits} = \log_2\left(\frac{512}{1}\right) = 9$$
$$\text{Offset bits} = \log_2(64) = 6$$
$$\text{Tag bits} = 32 - (9 + 6) = 17$$

4. Calculate the number of bits required for the *index*, *offset*, and *tag* for a **32 KiB** cache with **2048 lines** that is **4-way associative**.

$L = 2048$ (given). $W = 4$. $B = 32\text{KiB}/2048 = 16\text{B}$ (cache size over line size).

$$\text{Index bits} = \log_2\left(\frac{2048}{4}\right) = 9$$
$$\text{Offset bits} = \log_2(16) = 4$$
$$\text{Tag bits} = 32 - (9 + 4) = 19$$