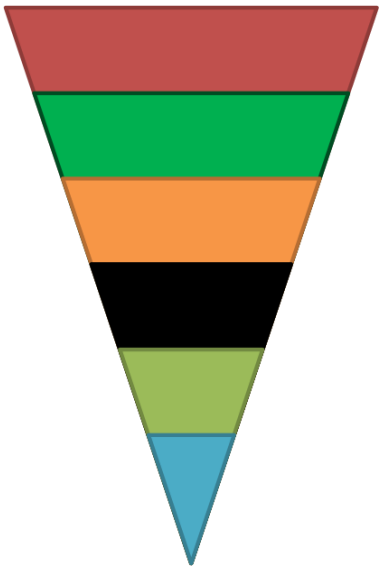
1. (3 points) Label each of the levels of the DRAM subsystem organization pyramid.



- Channel
- DIMM (Dual Inline Memory Module)
- Rank
- Chip
- Bank
- Row/Column

2. (3 points) Given the following information, fill in the table
   - **Row buffer hit:** only need to move data from row buffer to pins (~20 ns access time)
   - **Empty row buffer access:** must first read read the row, the move data from row buffer to pins (~40 ns access time)
   - **Row buffer conflict:** must first precharge the bitlines, then read the other row, the move data from row buffer to pins (~60 ns access time)

Requested	Time of Arrival	Time of Service	
		Open	Closed
X	0	40	40
Y	10	100	100
$X+1$	100	160	160
$X+2$	200	220	240
$Y+1$	250	310	300
$X+3$	300	370	360