CSCI 564: Homework 3

Name: _____ CWID: _____

For each of the following questions, please show all of your work, and explain your answers.

Key Terms

- *Aliasing* — the mapping of two or more branches to the same entry in the branch predictor data structure.
- *Negative interference* — the branch prediction rate of either or both aliased branches is reduced from what they would have been without aliasing.
- *Positive interference* — The branch prediction rate for either or both aliased branches is increased from what they would have been without aliasing.

1. The size of the branch predictor can affect the amount of aliasing (two branches mapping to the same entry in a branch prediction table) between branches. While this sort of aliasing usually results in negative interference, it can sometimes result in positive interference.

   (a) (10 points) Describe a branch T-NT (taken, not-taken) pattern for two branches for which aliasing will result in *negative* interference.

   (b) (10 points) Describe a branch T-NT (taken, not-taken) pattern for two branches for which aliasing will result in *positive* interference.

   (c) (5 points) Why is it that aliasing usually results in *negative* interference?

2. Assume we have a machine with a typical MIPS 5-stage pipeline that uses branch prediction *without* branch delay slots and has a branch misprediction penalty of three cycles. One in every five instructions is a branch for a certain program, of which 80% are predicted correctly by our branch predictor. Assume all non-branch instructions have a CPI of 1.

   (a) (10 points) How many cycles would it take to execute n instructions?

   (b) (15 points) Now, imagine we instead have a Pentium 4 which has a 20-stage pipeline. Because of this, the branch misprediction penalty is now a staggering 19 cycles! What would your branch prediction rate have to be such that it has the same performance as the MIPS machine from (a)?