1. Consider this 8-stage pipeline: IF | DE | RR | AL | AL | DM | DM | RW

For each of the following pairs of instructions, how many stalls will the second instruction experience without bypassing? With bypassing?

```
1 ADD R1 + R2 -> R3
```

```
1 LD [R1] -> R2
```

```
1 LD [R1] -> R2
```

```
1 LD [R1] -> R2
```

² ADD R3 + R4 -> R5

² ADD R2 + R3 -> R4

² SD [R2] <- R3

² SD [R3] <- R2